REMARKS

Claims 1–20 are pending in the present application.

Claim 7 was amended herein to alter the dependence of that claim, correcting an antecedent basis defect.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, Second Paragraph (Definiteness)

Claims 1–20 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. This rejection is respectfully traversed.

The standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope--that is, whether one skilled in the art would understand the bounds of the claim when read in light of the specification. MPEP § 2173.02, p.2100-205 (8th ed. rev. 2 May 2004). The claim is not indefinite if one skilled in the art would have no particular difficulty in determining whether the feature has been implemented. *Id.*

With respect to claims 1, 8 and 15, the Office Action states that "[I]t is not clear how the generated fold-status information is used." However, the claims themselves recites that the fold-status information "indicat[es] whether the successive entries contain two or more instructions which may be folded." As taught in the specification, the fold-status information indicates whether successive entries contain none, two or three instructions that may be folded and, if the entries

contain at least two instructions that may be folded, the byte boundaries for the first and second (and potentially third) instructions that may be folded. Specification, page 16. This information is employed by the main instruction decoder to immediately whether the instructions may be folded and, if so, how, so that an appropriate "folded" instruction may be passed to the execution unit:

> Whatever the case, the main instruction decoder 104 uses the five fold-status bits associated with the first byte within the instruction fetch buffer stack 202 to immediately determine whether folding can be performed, the number of instructions to be folded, and the byte boundaries of instructions to be folded. The instruction decoder 104 then generates control information to be passed to subsequent pipeline stages much more quickly than if the instruction decoder 104 first had to determine whether folding could be performed, and the instruction boundaries for instructions to be folded.

Specification, pages 19–20. Thus, those skilled in the art would have no particular difficulty in determining, in light of the specification, how the generated fold-status is employed.

Therefore, the rejection of claims 1–20 under 35 U.S.C. § 112, second paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 1, 5, 8, 12, 15 and 19 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,237,086 to *Koppala et al.* This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131, p. 2100-73 (8th ed. rev. 2 May 2004).

Independent claims 1, 8 and 15 each recited fold-status information "indicating whether the

successive entries contain two or more instructions which may be folded." Such a feature is not found in the cited reference. The cited portion of *Koppala et al* relates to signals indicating how many instructions were folded, not whether and how instructions may be folded:

> Folding logic circuit 2530 can also generate signals to indicate how many instructions were folded, i.e. combined into a group. Thus, signal FOLD2 indicates a two-instruction instruction group, signal FOLD3 indicates a three-instruction instruction group, and signal FOLD4 indicates a four-instruction instruction group.

Koppala et al, column 20, lines 14–19. The signals in *Koppala et al* thus correspond to the shift count signal transmitted in the present invention by the main instruction decoder to the instruction fetch buffer for removal of folded, completed instructions, NOT to the fold-status information generated by the fold decoders and stored in the instruction fetch buffer stack with the corresponding entries.

Therefore, the rejection of claims 1, 5, 8, 12, 15 and 19 under 35 U.S.C. § 103 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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